KORG®

PROGRAMMABLE SUPER SECTION

SERVICE MANUAL PSS-50

CONTENTS

KEIO ELECTRONIC LABORATORY CORPORATION
TOKYO/JAPAN

KORG® KEIO ELECTRONIC LABORATORY CORP.
15-12, Shimotakaido 1-chome, Suginami-ku, Tokyo 168

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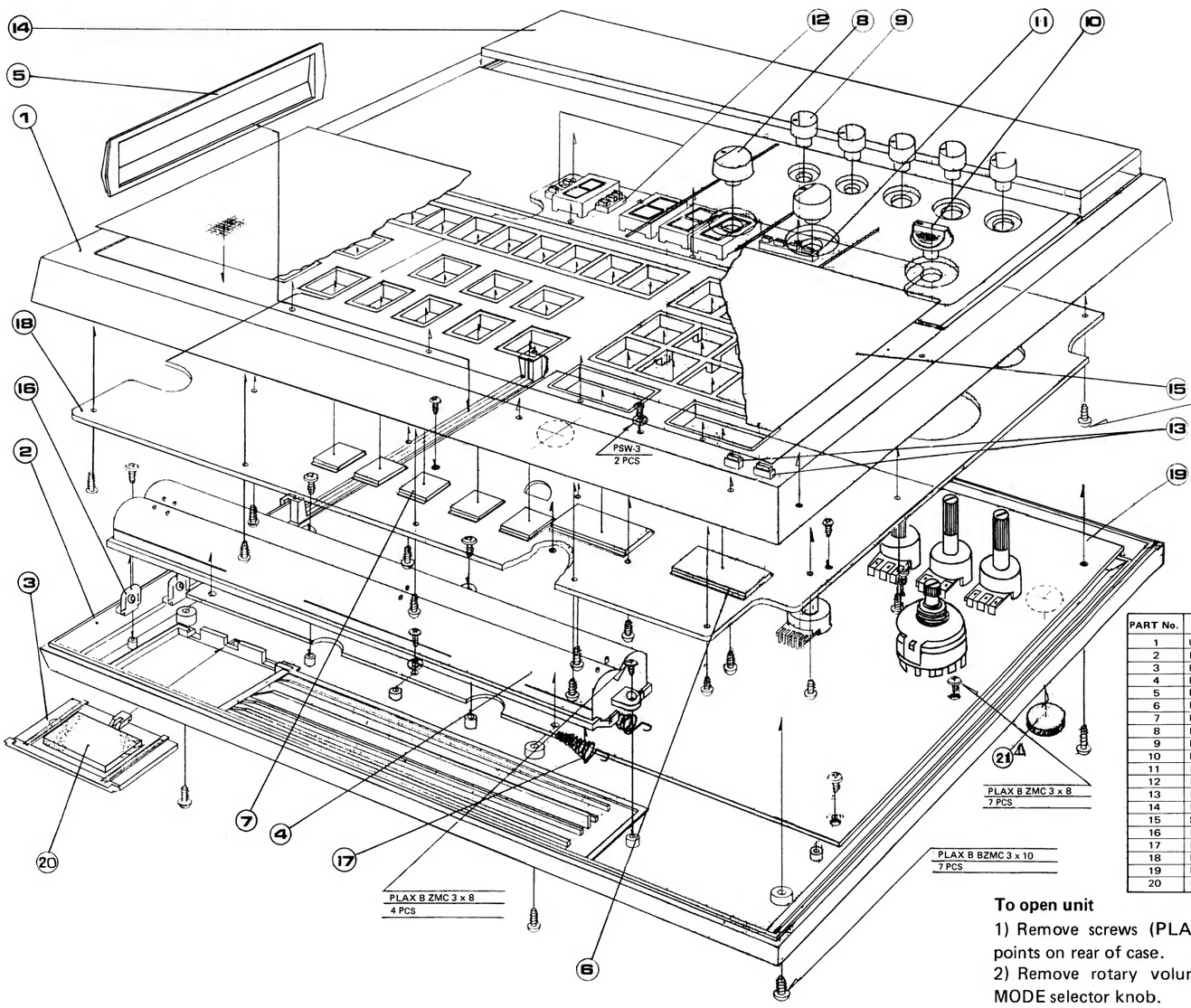
1. SPECIFICATIONS

- Tone generators: RHYTHM x 8 (bass drum, snare drum, rim shot, open high-hat, closed high-hat, high tom, low tom, hand-claps)
  BASS (electric bass)
  ACCOMPANIMENT (piano; electric piano, honky-tonk piano, distortion guitar, acoustic guitar, electric guitar, jazz guitar, cray, banjo, brass, synthesizer, organ, strings)
- Backup pattern: 48 Patterns (8 beat I-II, 16 beat I-II, new wave, electro pop, disco I-II, rock'n roll, boogie, ballad I-II, hard rock I-II-III, heavy metal, jazz waltz, 4 beat I-II, big band, fusion I-II-III-IV, bossa nova, samba, cha-cha, mambo, merengue, latin rock, reggae I-II, 2 beat, 3 beat, march, folk, country, blue grass, shuffle I-II, break & ending x 8)
- Arrangeable area: 16 Patterns
- Chord: Maj, m, m^6, m^7, m^9, 6, 7, Maj^7, 9, dim, Aug, sus 4 on each root (C–B)
- Memory bank: Song memory x 8 (maximum 80 bars/bank), Song chain (maximum 16 steps)
- Display: Chord name, Song/Pattern number, step number, bar number, battery check, tuning note, tape mode, conductor
- Mixer: Rhythm volume, Bass volume, Accompaniment volume, External input volume, Stereo volume
- Master volume: MIN. – MAX.
- Tempo: SLOW – FAST
- Power/mode selector: POWER OFF, BATT CHECK, TUNE, SONG CHAIN, PLAY, WRITE, ARRANGE
- Number keys: Pattern/Song (1 – 8)
- Song memory access: Chord, Pattern
- Function: Clear/All clear, Enter, Start/Stop, Count start/Rhythm fill in
- Key transpose: 0, +1 – +6, -1 – -5
- Key: END, INS, DEL, 1ST STEP, ◄, ►, LAST STEP
- Arrange key: ARRANGEABLE AREA 71 – 88, COPY, FILL IN, RHYTHM, ACC., BASS
- Tape interface: SAVE, LOAD, VERIFY, CANCEL
- Tune: ±50 sents
- Input selector: MIC, INST, LINE
- Tape switch: DISABLE/LINE IN, LINE OUT, EARPHONE, MIC OUT
- Input jacks: EXT IN, FROM TAPE, DC IN, START/STOP (⏚GND) FILL IN (⏚GND)
- Output jacks: OUTPUT (R/MIX, L), PHONES, TO TAPE
- Power supply: UM3 x 8/ DC 9V (AC adaptor)
- Dimensions: 310(W) x 210(D) x 50(H) mm
- Weight: 1.25kg (with battery)
- Accessories: AC adaptor, Connection cord (2.5m x 1), Batteries (SUM3 x 8)

PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
	BATTERY TERMINALs			
64905300	(+) Plus KOC-C40503			2
64905400	(—) Minus KOC-C40504			2
	SCREWs, WASHERs (Please refer to structural diagram)			
74530308	PLAX B ZMC 3x8			33
74560310	PLAX B BZMC 3x10			7
78690300	PSW 3			2
	INNER CARTON BOXes			
80020500	PSS-50			1
80220500	PSS-50 Packing R/L set			1

2. STRUCTURAL DIAGRAM

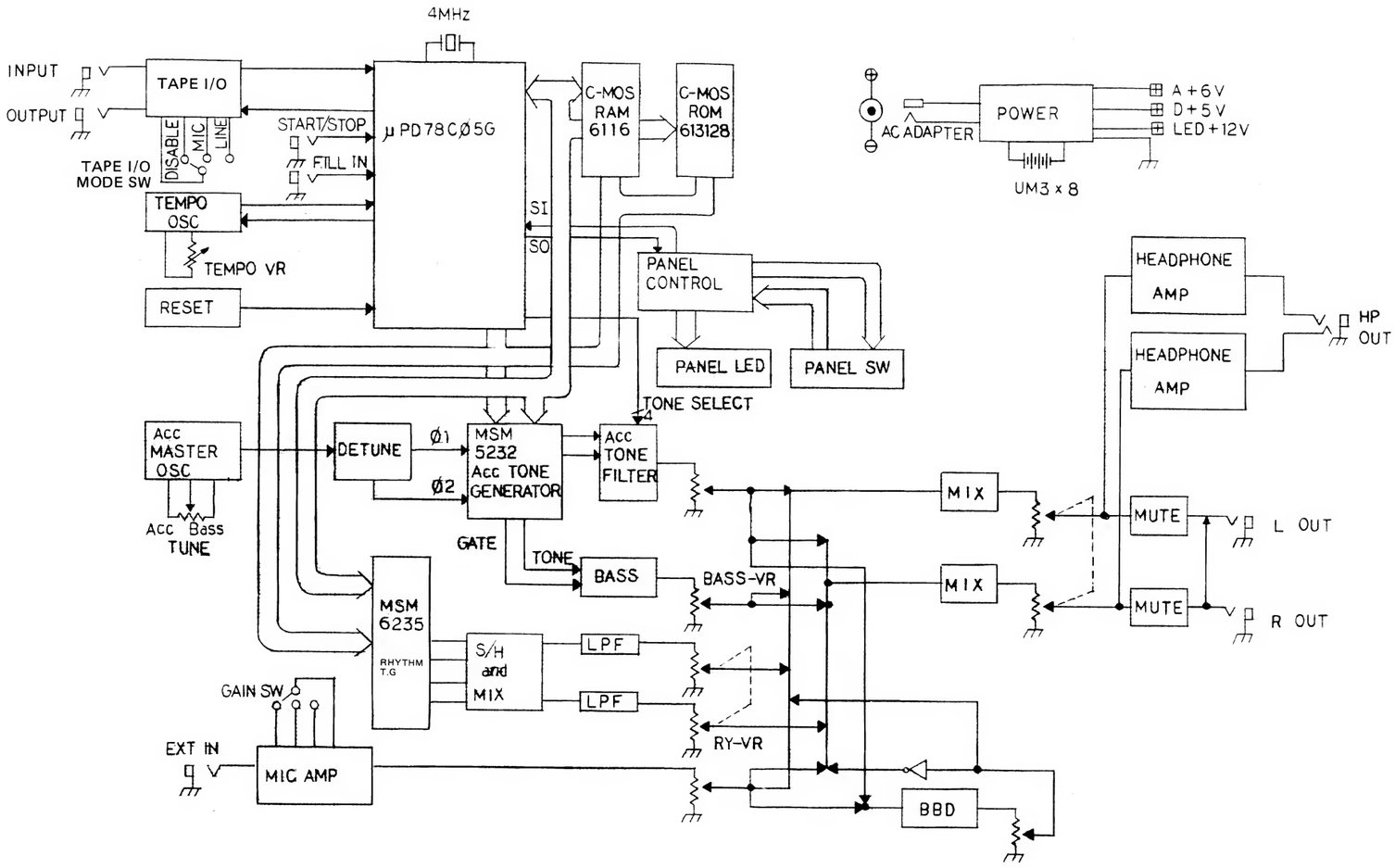


PART No.	PART NAME	PART CODE
1	UPPER CASE	64617200
2	LOWER CASE	64617300
3	BATTERY COVER	64617500
4	BATTERY HOLDER	64617400
5	PLASTIC COVER	64617600
6	PUSH SW KNOB (BIG)	62012900
7	PUSH SW KNOB (SMALL)	62012901
8	ROTARY VR KNOB (BIG)	62013100
9	ROTARY VR KNOB (SMALL)	62013101
10	MODE SW KNOB	62013000
11	LED SPACER (A)	64617700
12	LED SPACER (B)	64617701
13	LED SPACER (C)	64617702
14	DISPLAY COVER	64617800
15	SW OVERLAY SHEET	64617900
16	BATTERY TERMINAL (PLUS)	64905300
17	BATTERY TERMINAL (MINUS)	64905400
18	P.C. BOARD (KLM-563)	
19	P.C. BOARD (KLM-562)	
20	BATTERY CUSHION	50005300

To open unit

1) Remove screws (PLAX B BZMC 3 x 10) from seven points on rear of case.

2) Remove rotary volume knobs (large and small) and MODE selector knob.



PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
	HARNESSes			
47041000	HNS-310			1
47041100	HNS-311			1
	CONNECTOR TOPs			
47130400	B4B-XHA	KLM-562		1
47130900	B9B-XHA			1
	CONNECTOR SIDE			
47230900	S9B-XHA	KLM-563		1
	IC SOCKET			
48005282	28P C472811	KLM-562		2
	BATTERY CUSHION			
50005300	KOC-F40218			1
	RUBBER FEET			
50009100	KOC-F40296			2
	BATTERY			
52000300	SUM-3DG 1.5V			8
	JUMPER CORDs			
54515010	SMV2J-D7/0.16x3x70-P2.5-S5.0-F	KLM-562		1
54515020	SMV2J-D7/0.16x4x185-P2.5-S5.0-F			1
	BATTERY CAUTION SEAL			
58020101	KOC-F40301			1
	AUDIO CORD			
60201300	NEW 6.3φ Plug 2.5M			1

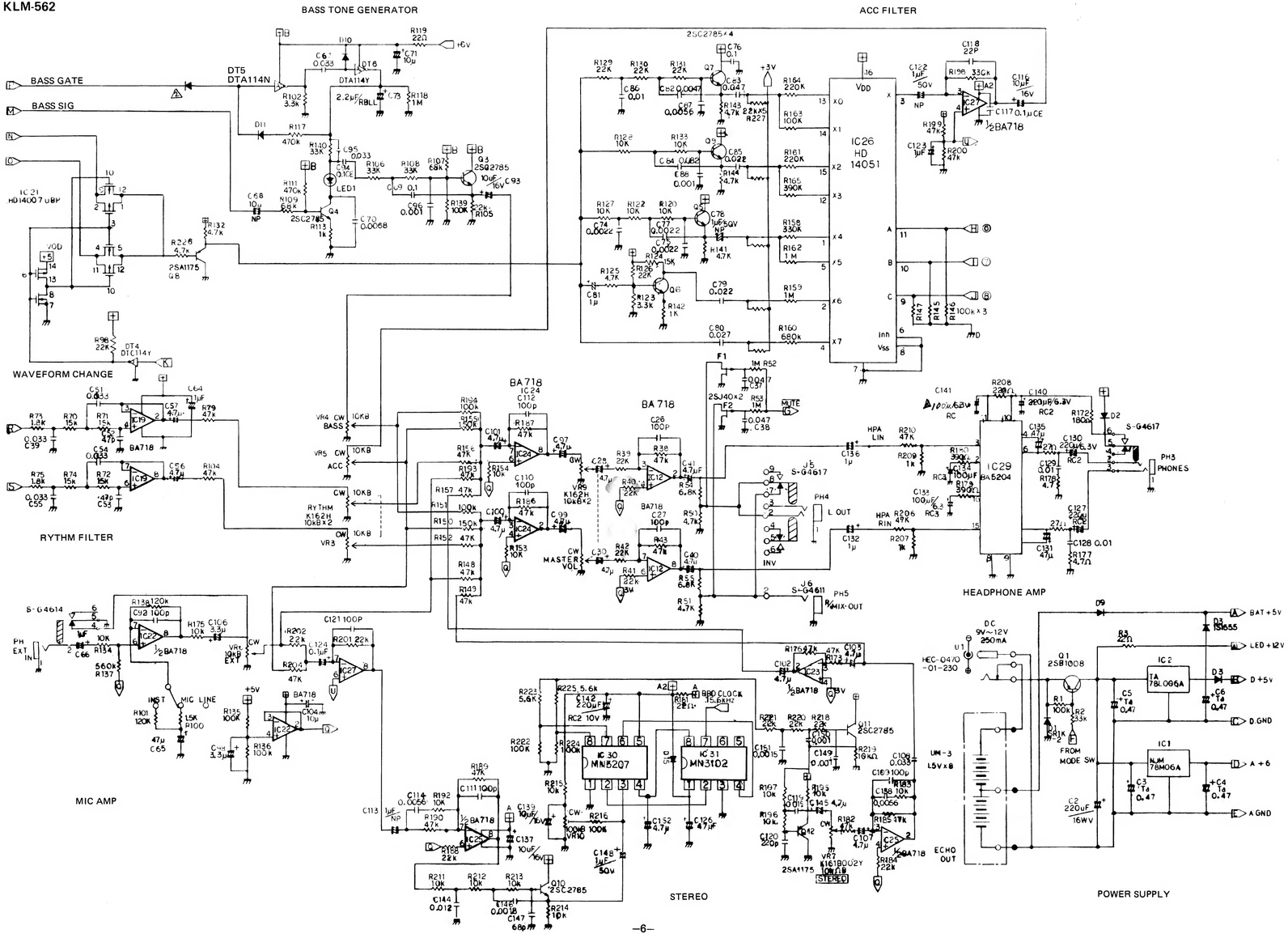
PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
	PUSH SW KNOBs			
62012900	Big KOC-E40146			2
62012901	Small KOC-E40147			37
	MODE SW KNOB			
62013000	KOC-E40154			1
	ROTARY VR KNOBs			
62013100	Big KOC-E40142			2
62013101	Small KOC-E40143			5
	CASEs			
64617200	Upper case KOC-E10010			1
64617300	Lower case KOC-E10011			1
	BATTERY HOLDER			
64617400	KOC-E30053			1
	BATTERY COVER			
64617500	KOC-E40145			1
	PLASTIC COVER			
64617600	KOC-E40148			1
	LED SPACERs			
64617700	A KOC-E40161	KLM-563		1
64617701	B KOC-E40162			2
64617702	C KOC-E40163			2
	DISPLAY COVER			
64617800	KOC-E30054			1
	SW OVERLAY SHEET			
64617900	KOC-E30055			1

PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
32003030	TC-40H151 P	KLM-563	IC3 8 line to 1 line data multiplexer	1
32003043	TC-40H032 P	KLM-562	IC7 Quadruple 2 input positive or gate	1
32003063	TC-40H393 P	KLM-563	IC4 Dual 4 bit binary counter	1
32004002	HD-14007 UBP	KLM-562	IC21 Dual complementary pair plus inverter	1
32004017	HD-14051 BP		IC26 8 channel analog multiplexer	1
32004019	HD-14049 UBP		IC5 Hex inverter	1
		KLM-563		1
32004028	HM-6116LP-4	KLM-562	IC14 RAM	1
32004064	HD-14040 BP		IC3 12 bit binary counter	1
32004065	HN613128 PD62		IC11 ROM	1
32006009	MSM-5232RS		IC18 Tone generator (Acc. Bass)	1
32006012	MSM-6235RS-01		IC13 Tone generator (Rhythm)	1
32007004	BA-718		Dual OP AMP	9
32007005	BA-823	KLM-563	IC1 8 bit serial in paralel out driver	1
32007006	BA-5204	KLM-562	IC29 Headphone AMP	1
32007007	BA-728		IC20 OP AMP	1
32009030	NJM-78L06A	KLM-562		1
32009031	NJM-78M06A			1
32012001	MB-3761 M		IC28 Reset	1
32021017	LM-393 N		IC17 Comparator	1
CERAMIC OSCILLATOR				
33501400	KBR-4.0MHz	KLm-562		1
P.C. BOARDs (without parts)				
34056200	KLM-562			1
34056300	KLM-563			1
SEMI-FIXED RESISTORs				
35121250	B5K	KLM-562	VR1 Pitch	1
35121410	B100K		VR10 BBD Bias	1
ROTARY VRs				
36017000	K162H0012-10KB	KLM-562	VR9 Master, VR3 Rhythm	2
36017100	K161B002Y-10KB		VR4, VR5, VR6, VR7	4
36017200	K161B002W-500KC		VR8 Tempo	1
36017300	K121K0Z05-30KB		VR2 Tune	1
ROTARY SW				
37002900	SRM1017150	KLM-562	SW3 Mode SW	1

PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
SLIDE SW				
37304800	SSB-323055	KLM-562	SW1 Tape I/O	2
PUSH SW				
37505400	EVQ-QS307K	KLM-563		39
COIL				
40201000	50UH KL-001	KLM-562	L1	1
AC ADAPTERs				
40502600	KAC-301 100V		100V	1
40502700	KAC-302 UNI/117V		UNI	1
			117 2P	1
40502800	KAC-303 JAM/CSA		JAM	1
40503000	KAC-305 240AU		240 AU	1
40503100	KAC-306 240GE		240 GE	1
			240 RM	1
40503200	KAC-307 240AF		240 AF	1
40503300	KAC-308 220GE/ SCHANDINAVIA		220 GE	1
			220 SE	1
			DEMKO	1
			SEMKO	1
			NEMKO	1
			GAF	1
			FEMKO	1
PHONE JACKs				
45001400	SG-4611 #01	KLM-562		3
45001500	SG-4614 #01			1
45001600	SG-4617 #01			2
DC INPUT JACK				
45400300	HEC-0470-01-230	KLM-562		1
MINI-PHONE JACK				
45400900	HSJ-0786-01-010 3.5φ	KLM-562		2

4. CIRCUIT DIAGRAM KLM-562

KLM-562

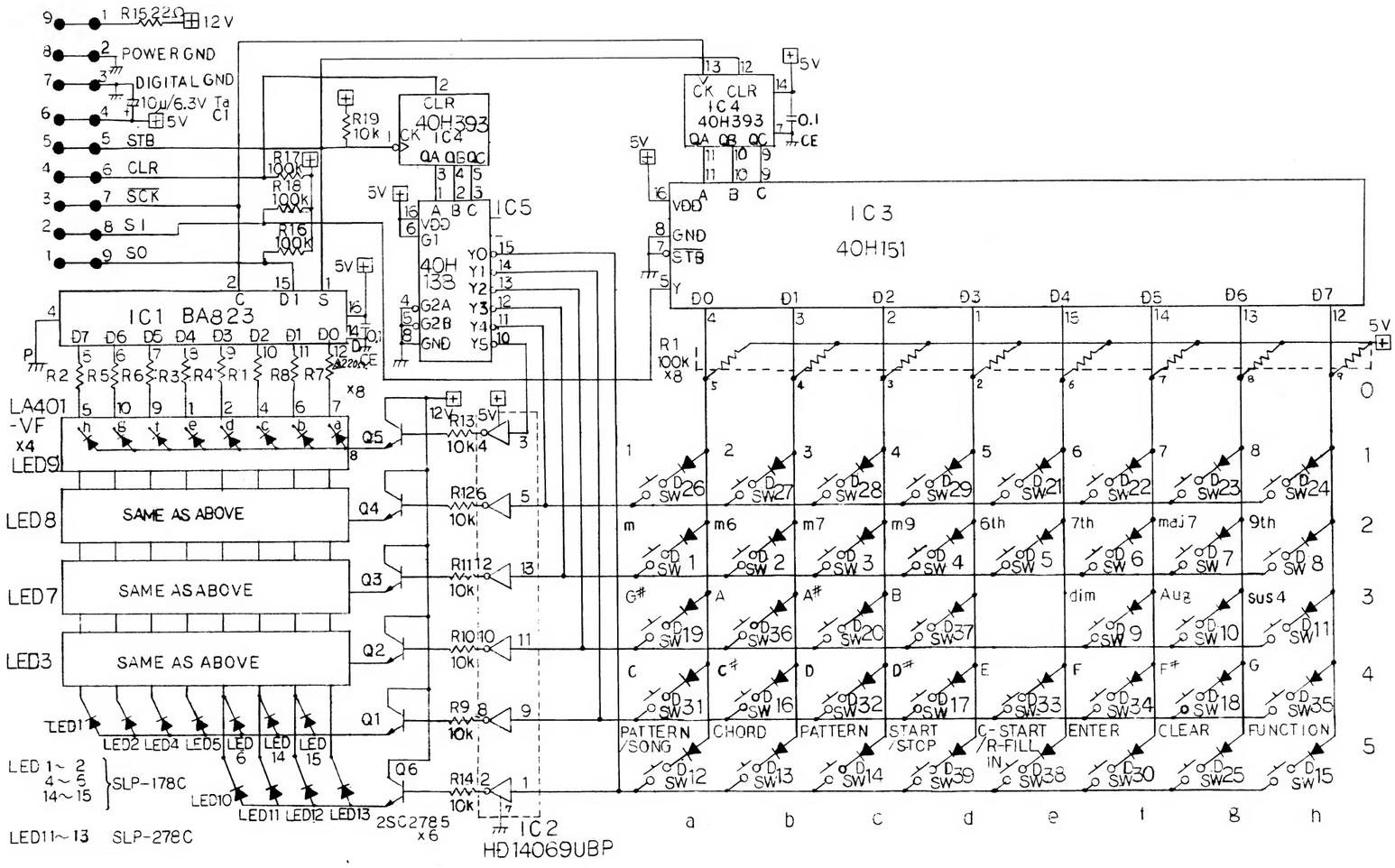


PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
			STYROL CAPACITORS	
20502415	50V GT 1500PF	KLM-562		2
20503247	50V JT 47PF			2
20503268	50V JT 68PF			1
20503315	50V JT 150PF			1
20503322	50V JT 220PF			1
			CERAMIC CAPACITORS	
21442221	50V 22PF	KLM-562		3
21442470	50V 47PF			2
21443100	50V 100PF			8
21443470	50V 470PF			2
21446100	25V 0.1μF	KLM-563		7
				2
			TANTALUM CAPACITORS	
22407210	16V 10μF	KLM-563		1
22425010	35V 0.1μF	KLM-562		2
22425047	35V 0.47μF			4
			ELECTROLYTIC CAPACITORS	
23723410	6.3V 1000μF RC	KLM-562		1
25401247	6.3V 47μF RE.T2			3
25403210	16V 10μF RE.T2			11
25403247	16V 47μF RE.T2			1
25404147	25V 4.7μF RE.T2			19
25406010	50V 0.1μF RE.T2			3
25406110	50V 1μF RE.T2			7
25406133	50V 3.3μF RE.T2			2
25423247	16V 47μF RB-LL.T2			1
25426033	50V 0.33μF RB-LL.T2			1
25426110	50V 1μF RB-LL.T2			8
25426122	50V 2.2μF RB-LL.T2			1
25433322	16V 220μF REA-T2			1
25442322	4V 220μF RC2.T2			4
25451310	6.3V 100μF RC-3.T2			3
25463210	16V 10μF RBP.T2			1
25466110	50V 1μF RBP.T2			3

PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
			TRANSISTORs	
30100800	TR 2SB-1008	KLM-562		1
30400020	TR 2SA1175 K TN			3
30420020	TR 2SC2785 K TN			8
30420030		KLM-563		6
			DIGITAL TRANSISTORs	
30430010	DTA-114N T-93	KLM-562		1
30430030	DTA-114Y T-93			2
30430040	DTC-114Y T-93			4
			FET	
30460110	2SJ40-34-C	KLM-562		2
			DIODEs	
31001500	SR1K-2	KLM-562		1
31204100	LTZ-R15			1
31400100	1S1555 TP-3	KLM-563		10
		KLM-562		39
31401300	1SS-133 T-77			1
			LEDs	
31203600	SLP-178C	KLM-563		8
31203700	SLP-278C			3
31203800	LA401-VP K/L			4
			DOUBLE DIODE	
31430100	MC-931 TP	KLM-562		3
			ICs	
32001054	UPD78C05G	KLM-562	IC10 CPU	1
32002022	MN-3102		IC31 BBD driver	1
32002023	MN-3207		IC30 BBD	1
32003013	TC-40H004 P		IC8 Hex inverter	1
32003021	TC-40H074 P		IC6 Dual D type positive edge-triggered flip flop	1
32003026	TC-40H138 P	KLM-563	IC4 3 line to 8 line decoder	1
			IC12	1

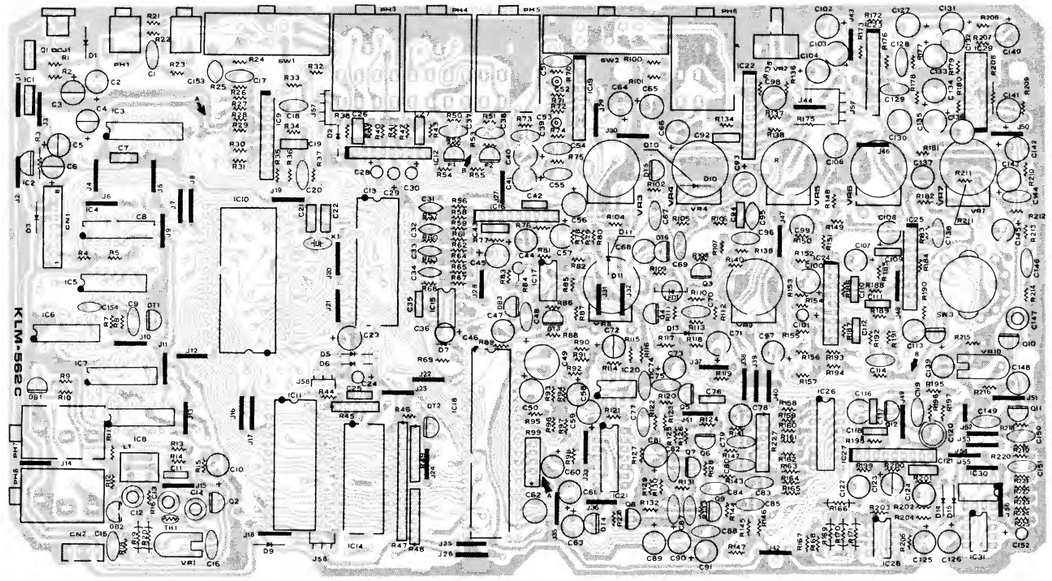
10. PARTS LIST

PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
	CARBON RESISTORs			
10413222	S1/4JYTP 22Ω	KLM-562		1
		KLM-563		1
10413322	S1/4JYTP 220Ω	KLM-562		1
		KLM-563		8
10413510	S1/4JYTP 10K	KLM-562		1
		KLM-563		7
10413610	S1/4JYTP 100K			4
10416147	1/6JTP 4.7Ω	KLM-562		2
10416215	1/6JTP 15Ω			1
10416222	1/6JTP 22Ω			2
10416227	1/6JTP 27Ω			2
10416268	1/6JTP 68Ω			1
10416310	1/6JTP 100Ω			1
10416318	1/6JTP 180Ω			1
10416339	1/6JTP 390Ω			2
10416410	1/6JTP 1.0K			8
10416412	1/6JTP 1.2K			1
10416415	1/6JTP 1.5K			1
10416418	1/6JTP 1.8K			2
10416422	1/6JTP 2.2K			2
10416433	1/6JTP 3.3K			2
10416447	1/6JTP 4.7K			9
10416456	1/6JTP 5.6K			2
10416468	1/6JTP 6.8K			3
10416482	1/6JTP 8.2K			0
10416510	1/6JTP 10K			27
10416515	1/6JTP 15K			5
10416522	1/6JTP 22K			29
10416527	1/6JTP 27K			1
10416530	1/6JTP 30K			1
10416533	1/6JTP 33K			4
10416547	1/6JTP 47K			28
10416568	1/6JTP 68K			4
10416610	1/6JTP 100K			24
10416612	1/6JTP 120K			2
10416615	1/6JTP 150K			6
10416618	1/6JTP 180K			2
10416622	1/6JTP 220K			2
10416633	1/6JTP 330K			10
10416639	1/6JTP 390K			2
10416647	1/6JTP 470K			4
10416656	1/6JTP 560K			1
10416668	1/6JTP 680K			1
10416682	1/6JTP 820K			1
10416710	1/6JTP 1.0M	KLM-562		6
10416722	1/6JTP 2.2M			2
	METAL FILM RESISTORs			
12415150	1/4TP 15.0K	KLM-562		1
12415536	1/4TP 53.6K			1
12416121	1/4TP 121K			2
12416332	1/4TP 332K			1
12416619	1/4TP 619K			1
	BLOCK RESISTORs			
13504447	RKC1/8B4J 4.7K	KLM-562		1
13505522	RKC1/8B5J 22K			1
13505610	RKC1/8B5J 100K			2
13508610	RKC1/8B8J 100K	KLM-563		1
13603610	RKC1/8B3DJ 100K	KLM-562		1
13611610	RKC1/8B11DJ 100K			1
	THERMISTOR			
18032310	TD5-A110DA	KLM-562		1
	MYLAR CAPACITORs			
20402410	50V 0.001μF K	KLM-562		11
20402415	50V 0.0015μF K			1
20402418	50V 0.0018μF K			1
20402422	50V 0.0022μF K			3
20402433	50V 0.0033μF K			1
20402447	50V 0.0047μF K			2
20402456	50V 0.0056μF K			3
20402468	50V 0.0068μF K			1
20402510	50V 0.01μF K			5
20402512	50V 0.012μF K			1
20402515	50V 0.015μF K			1
20402522	50V 0.022μF K			4
20402527	50V 0.027μF K			1
20402533	50V 0.033μF K			7
20402547	50V 0.047μF K			3
20402582	50V 0.082μF K			1
20402610	50V 0.1μF K			1

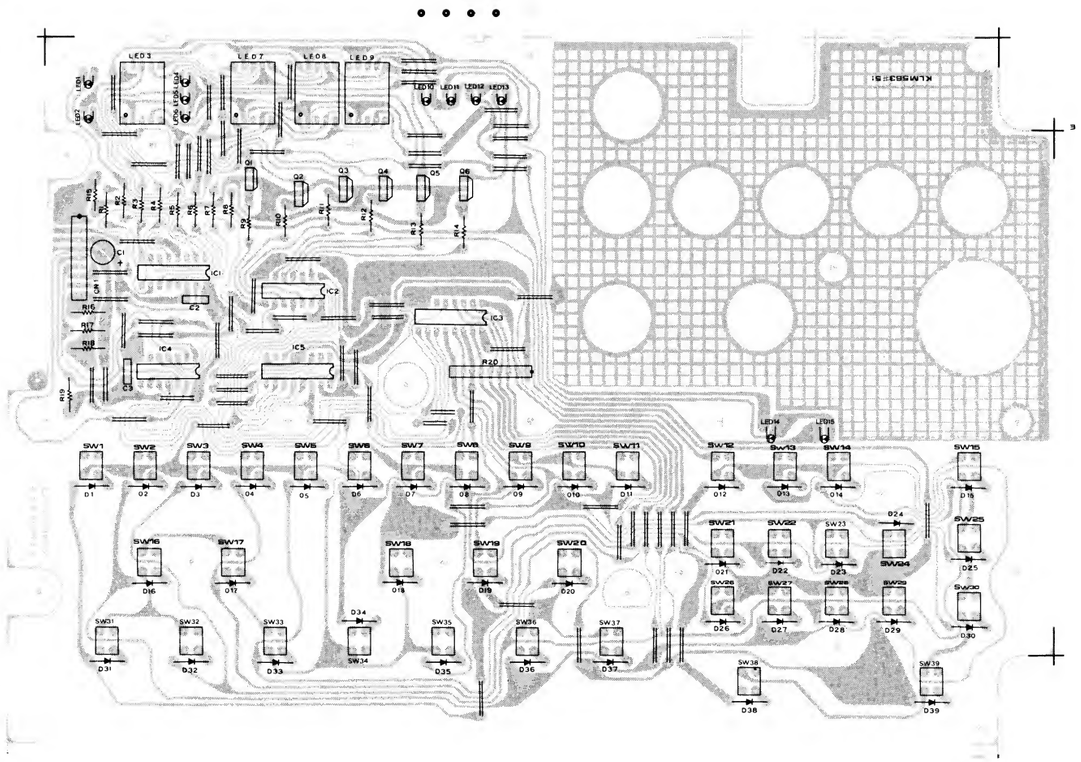


5. PC BOARD

KLM-562

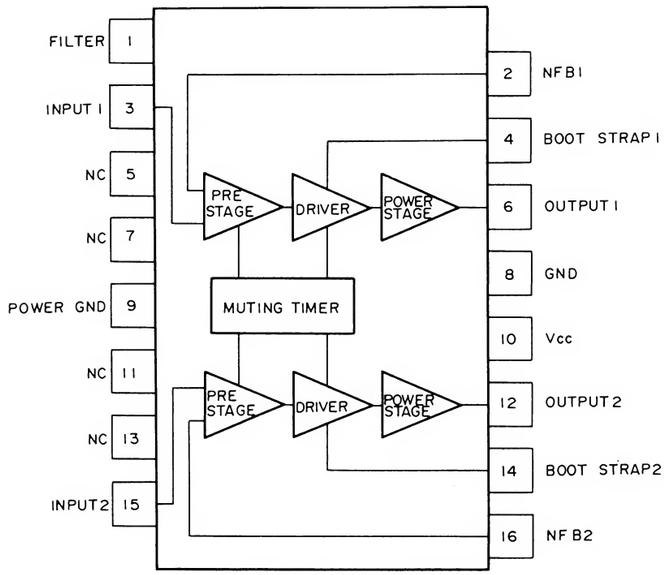


KLM-563

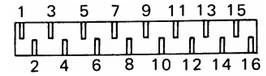


HEADPHONE AMP BA5204

BLOCK DIAGRAM

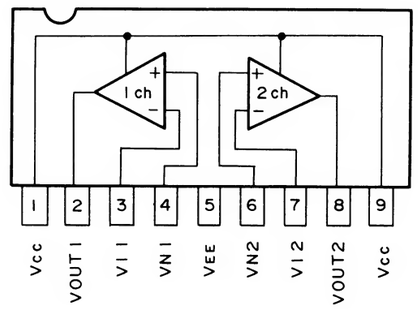


PIN CONFIGURATION



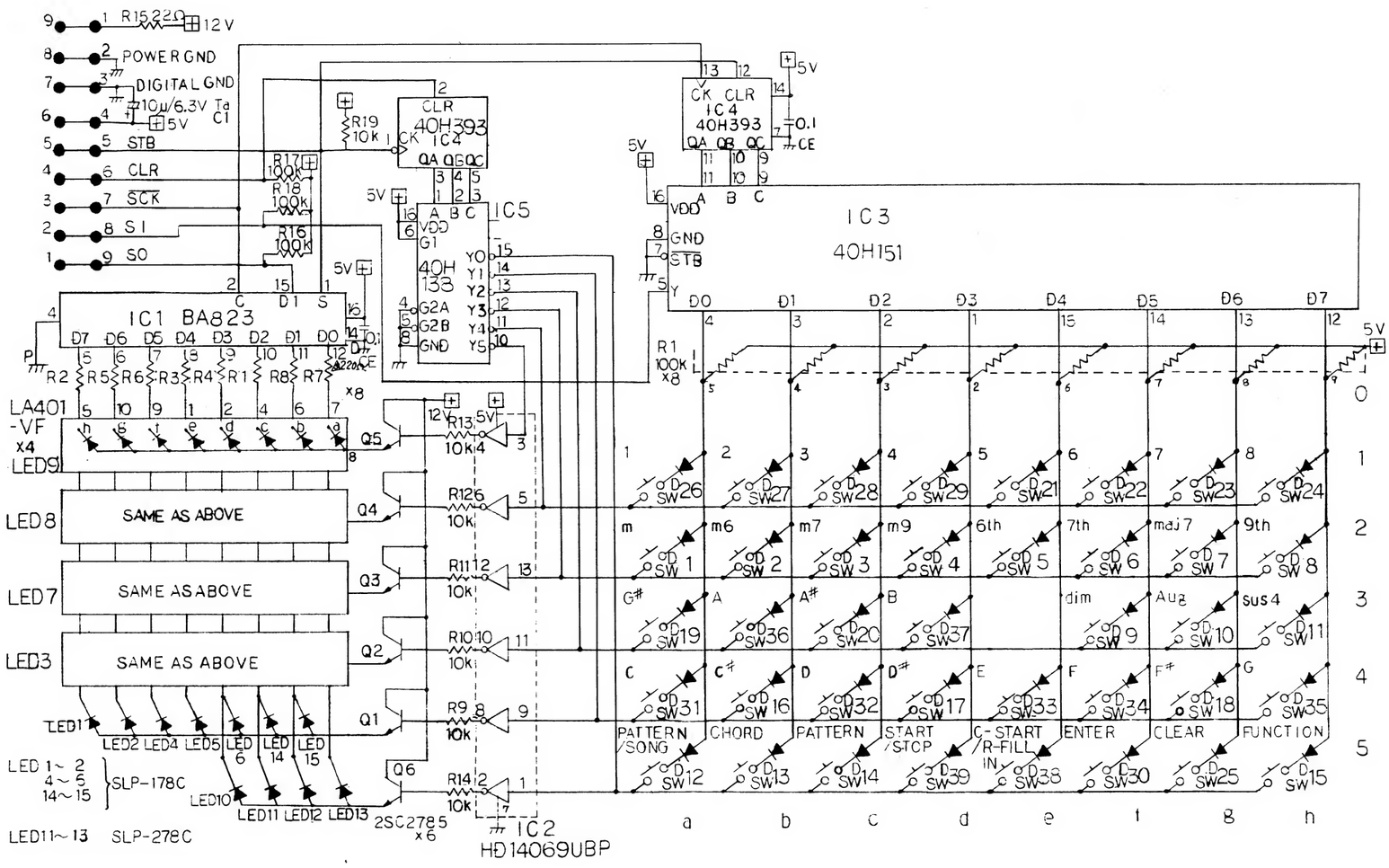
DUAL OP AMP BA718

BLOCK DIAGRAM



10. PARTS LIST

PARTS CODE	PARTS NAME SPECIFICATIONS	P.C. BOARD	IDENTIFICATION NO. FUNCTION	Q'TY
	CARBON RESISTORs			
10413222	S1/4JYTP 22Ω	KLM-562		1
		KLM-563		1
10413322	S1/4JYTP 220Ω	KLM-562		1
		KLM-563		8
10413510	S1/4JYTP 10K	KLM-562		1
		KLM-563		7
10413610	S1/4JYTP 100K			4
10416147	1/6JTP 4.7Ω	KLM-562		2
10416215	1/6JTP 15Ω			1
10416222	1/6JTP 22Ω			2
10416227	1/6JTP 27Ω			2
10416268	1/6JTP 68Ω			1
10416310	1/6JTP 100Ω			1
10416318	1/6JTP 180Ω			1
10416339	1/6JTP 390Ω			2
10416410	1/6JTP 1.0K			8
10416412	1/6JTP 1.2K			1
10416415	1/6JTP 1.5K			1
10416418	1/6JTP 1.8K			2
10416422	1/6JTP 2.2K			2
10416433	1/6JTP 3.3K			2
10416447	1/6JTP 4.7K			9
10416456	1/6JTP 5.6K			2
10416468	1/6JTP 6.8K			3
10416482	1/6JTP 8.2K			0
10416510	1/6JTP 10K			27
10416515	1/6JTP 15K			5
10416522	1/6JTP 22K			29
10416527	1/6JTP 27K			1
10416530	1/6JTP 30K			1
10416533	1/6JTP 33K			4
10416547	1/6JTP 47K			28
10416568	1/6JTP 68K			4
10416610	1/6JTP 100K			24
10416612	1/6JTP 120K			2
10416615	1/6JTP 150K			6
10416618	1/6JTP 180K			2
10416622	1/6JTP 220K			2
10416633	1/6JTP 330K			10
10416639	1/6JTP 390K			2
10416647	1/6JTP 470K			4
10416656	1/6JTP 560K			1
10416668	1/6JTP 680K			1
10416682	1/6JTP 820K			1
10416710	1/6JTP 1.0M	KLM-562		6
10416722	1/6JTP 2.2M			2
	METAL FILM RESISTORs			
12415150	1/4TP 15.0K	KLM-562		1
12415536	1/4TP 53.6K			1
12416121	1/4TP 121K			2
12416332	1/4TP 332K			1
12416619	1/4TP 619K			1
	BLOCK RESISTORs			
13504447	RKC1/8B4J 4.7K	KLM-562		1
13505522	RKC1/8B5J 22K			1
13505610	RKC1/8B5J 100K			2
13508610	RKC1/8B8J 100K	KLM-563		1
13603610	RKC1/8B3DJ 100K	KLM-562		1
13611610	RKC1/8B11DJ 100K			1
	THERMISTOR			
18032310	TD5-A110DA	KLM-562		1
	MYLAR CAPACITORs			
20402410	50V 0.001μF K	KLM-562		11
20402415	50V 0.0015μF K			1
20402418	50V 0.0018μF K			1
20402422	50V 0.0022μF K			3
20402433	50V 0.0033μF K			1
20402447	50V 0.0047μF K			2
20402456	50V 0.0056μF K			3
20402468	50V 0.0068μF K			1
20402510	50V 0.01μF K			5
20402512	50V 0.012μF K			1
20402515	50V 0.015μF K			1
20402522	50V 0.022μF K			4
20402527	50V 0.027μF K			1
20402533	50V 0.033μF K			7
20402547	50V 0.047μF K			3
20402582	50V 0.082μF K			1
20402610	50V 0.1μF K			1



Terminal functions

$\overline{\text{RESET}}$ input.
Resets LSI when at low level. Needs minimum of one clock pulse width.

CLK (clock) input.
Clock input used for internal timing. Takes frequency sixteen times sampling frequency.

$\overline{\text{WR}}$ (write) input.
Writes control data from CPU (via data bus) when at low level.

$\overline{\text{RD}}$ (read).
If this input is low level then the CPU can read status data from this chip.

$\overline{\text{CS}}$ (chip select).
This LSI is enabled by a low level input from the device select signal directly over the address bus or via a decoder. This LSI can be accessed when the signal is at high level.

D0–D7 (data bus) IO tristate.
This 8-bit 3-state bidirectional data bus connects to the microcomputer system data bus.
Active when $\overline{\text{CS}}$="HIGH".
High impedance when $\overline{\text{CS}}$="LOW".

$\overline{\text{CASIN}}$ (cascade input);
$\overline{\text{CASOUT}}$ (cascade output).

These terminals are used when several LSIs are connected in a cascade series. If the chip is being used independently then CASIN should be set to LOW.
Several chips may be connected as shown in the diagram here.

These terminals are only effective for channel 0.

OUT 0–3 (signal output).
Time shared output sigansl for each channel.

MIXOUT (mixed signal output).
Time shared signal output.

MIXIN (mixed signal input).
A MIXOUT signal can be buffered and dropped to low impedance, then input to this terminal.

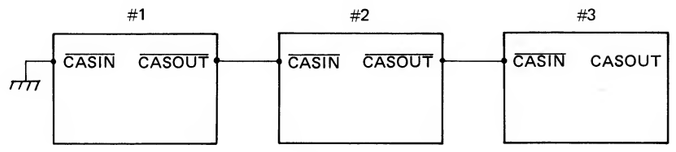
TEST.
Self test using positive logic. Normally connected to DVss.

AVPD Analog VPD.

AVss Analog Vss.
Power supply for DAC.

DVDD Digital VPD.
+5V.

DVss Digital Vss.
GND.



6. CIRCUIT DESCRIPTIONS

1. KLM-562 circuit description.

This is made up of digital circuitry (basic system based on uPD78C05 8-bit microprocessor), analog circuitry (ACC filters, bass tone generator, headphone amp, external input amp, and stereo circuit), and the power supply circuit.

1) CPU uPD78C05

All PSS-50 operations are processed by this CPU. Simple explanations of the functions of each port are found below.
Port A is an 8-bit output port.
PA 0 . . . This single bit controls the strings detune circuit.
("L" during ACC strings selection; otherwise "H".)

PA 1-3 . . . These 3 bits control ACC (accompaniment) filter switching. (Switching of IC26, 14051.)
The ACC pattern is fixed in the PSS-50. In case of a malfunction or when checking, refer to chart 1.

PA 4 . . . This single bit switches the ACC waveform. (The tone generator has two kinds of waveform: ACC1 is for strings, brass, etc.; ACC2 is for piano, organ, and related sounds.)

Chart 1

Pattern No.	PA1 (Pin 34)	PA2 (Pin 35)	PA3 (Pin 36)	PA4 (Pin 37)	Pattern No.	PA1 (Pin 34)	PA2 (Pin 35)	PA3 (Pin 36)	PA4 (Pin 37)
11	H	H	H	H	41	L	L	L	H
12	H	L	L	L	42	H	L	L	L
13	H	H	H	H	43	L	L	H	H
14	H	L	H	H	44	H	H	L	H
15	L	H	H	H	45	H	H	L	H
16	L	L	H	L	46	H	H	L	H
17	H	H	L	H	47	H	H	L	H
18	L	L	H	H	48	H	H	L	L
21	H	L	L	H	51	L	L	H	H
22	L	L	H	H	52	L	L	L	H
23	L	L	H	H	53	L	L	H	H
24	L	L	L	L	54	H	H	H	H
25	L	H	H	H	55	H	H	H	H
26	L	H	H	H	56	L	H	L	H
27	H	H	H	H	57	L	L	H	H
28	L	H	H	H	58	L	L	H	H
31	H	L	L	L	61	L	L	H	H
32	H	L	L	L	62	L	L	H	H
33	H	L	L	L	63	L	L	H	H
34	L	L	H	H	64	L	L	H	H
35	L	L	H	H	65	L	L	H	H
36	H	H	L	H	66	L	L	H	H
37	H	H	L	H	67	L	L	H	H
38	L	L	H	H	68	L	L	H	H

PA 5 . . . NC
PA 6 . . . STB signal output.
PA 7 . . . CLR signal output.

} With SCK these control serial data I/O (SI, SO) timing.

The PB ports are I/O ports with the following main functions.

PB 0 . . . Tempo oscillator reset output. The PSS-50 tempo oscillator uses the CPU in its feedback loop to enable control of start/stop and other timing functions.

PB 1, PB 2 } Tape interface output
PB 3 . . . NC
PB 4 . . . NC
PB 5 . . . Tape interface input.
PB 6 . . . Tape interface switch position input.
PB 7 . . . Single bit input for battery check determination (Gd or nG display). Input is L when battery has worn down.

The PC port inputs are interpreted as shown in the chart below. This 4-bit code is determined by mode switch position. The unit then runs the corresponding program and controls LED display. Therefore, check CPU PC ports PC0-PC3 if a problem is related to the LED display.

MODE SWITCH CHECK LIST

Port C \ Mode SW	Battery check	Tune	Song chain	Play	Write	Arrange
PC 0 (Pin 23)	H	L	H	H	H	H
PC 1 (Pin 22)	L	H	L	H	H	H
PC 2 (Pin 21)	H	L	H	L	H	H
PC 3 (Pin 20)	H	H	L	H	L	H

As for the two other bits (PC4, PC5), one bit is for foot switch start/stop control and the other is for rhythm fill-in control.

CAUTION:
Unit goes into tape mode when PB6 is high (H) regardless of status of PC0-PC3.

2) ROM: HN613128P D62.
A 128kbit CMOS mask ROM.

3) RAM: HM6116LP-4.
2048-word x 8-bit static CMOS RAM.

4) Tone generator.

MSM-5232: For ACC and Bass generation.
MSM-6235: For rhythm section generation.

For more details please see the reference data.

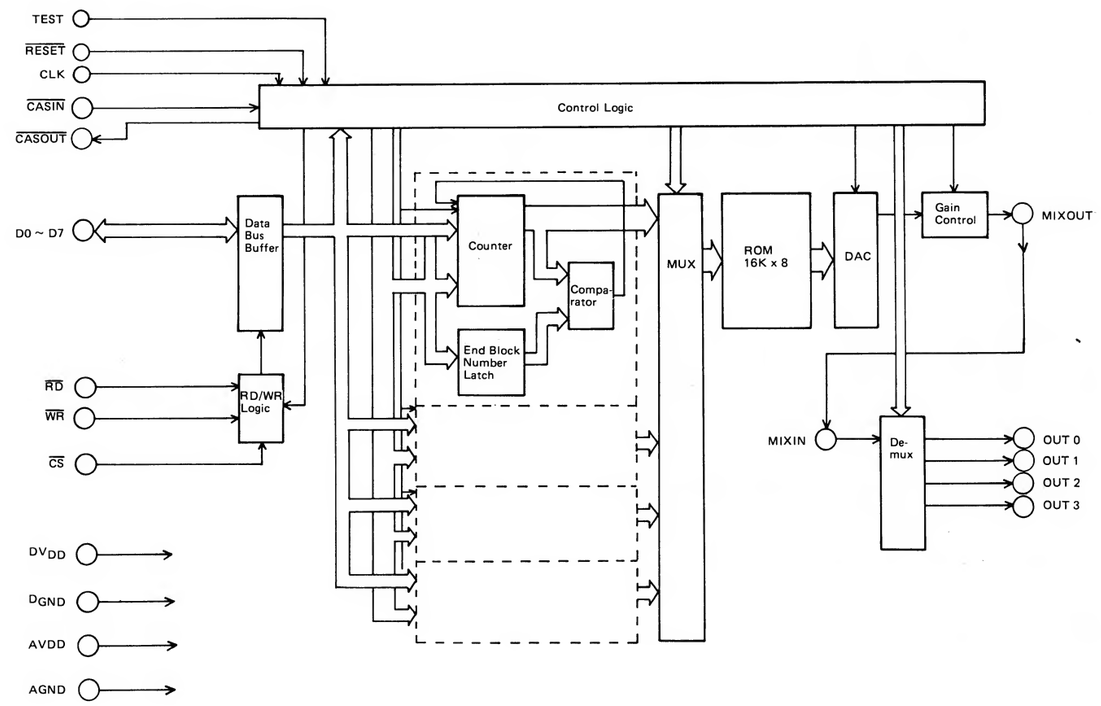
2. KLM-563 functions.

KLM-563 consists of a switch matrix circuit and 7-segment LED display circuit.
Connections (number of harnesses) are reduced by using IC1 (BA823), an 8-bit serial-in parallel-out driver, and IC3 (40H151), an 8-line to 1-line data multiplexer.
IC1 syncs 8-bit serial data from the CPU with the SCK signal, converts it into parallel data, and time shares to light the LEDs. The CPU STB signal is used as the IC4 (binary counter) clock and supplied by IC5 (3 to 8 decoder) to the switch matrix (SW matrix).
This permits detection of switch positions. Switch position data is output by the IC3 5-pin as serial data and read into the CPU.

TONE GENERATOR MSM6235RS

MSM6235RS is a sound generator IC that uses PCM recorded instrument sounds in ROM and includes a DAC and 8-bit bus interface, all on one chip. It is controlled by a microprocessor and can output any four sounds at once out of a possible sixteen.

BLOCK DIAGRAM



PIN CONFIGURATION

28 pin Lead Plastic DIP

RESET	1	28	DVDD
CLK	2	27	TEST
RD	3	26	NC
WR	4	25	OUT 0
CS	5	24	OUT 1
D0	6	23	OUT 2
D1	7	22	OUT 3
D2	8	21	NC
D3	9	20	MIXIN
D4	10	19	AVDD
D5	11	18	MIX OUT 2
D6	12	17	AVSS
D7	13	16	CASIN
DVSS	14	15	CASOUT

PIN NAMES

CS	CHIP SELECT
RD	READ
WR	WRITE
D0 ~ D7	DATA BUS (BI-DIRECTIONAL)
RESET	RESET
CLK	CLOCK
CASIN	CASCADE INPUT
CASOUT	CASCADE OUTPUT
MIXOUT	MIXED SIGNAL OUTPUT
MIXIN	MIXED SIGNAL INPUT
OUT0 ~ 3	SIGNAL OUTPUT
TEST	TEST

IC MSM5232RS SPECIFICATIONS

The MSM5232RS is a musical instrument tone generator IC that includes eight sets of scale generating frequency dividers and envelope generators with an 8-bit bus interface integrated on a single chip. It can simultaneously output eight sounds over a seven octave range under microprocessor control.

CHARACTERISTICS

- 2-group 4+4—tone polyphonic output.
  Each group has its own clock input, output bus, and control register, enabling rich, variegated sound operation.
- 7-octave range, plus noise output capability.
- Four foot length outputs: 2', 4', 8' and 16'.
- Built-in envelope generator.
  Sustained and attenuated envelope waveforms and variable attack and delay time constants.
- Interface for 8-bit microprocessor control.
- Built-in scale generating ROM converts key number into frequency divider data.
- CMOS IC means low power operation.

PIN FUNCTIONS

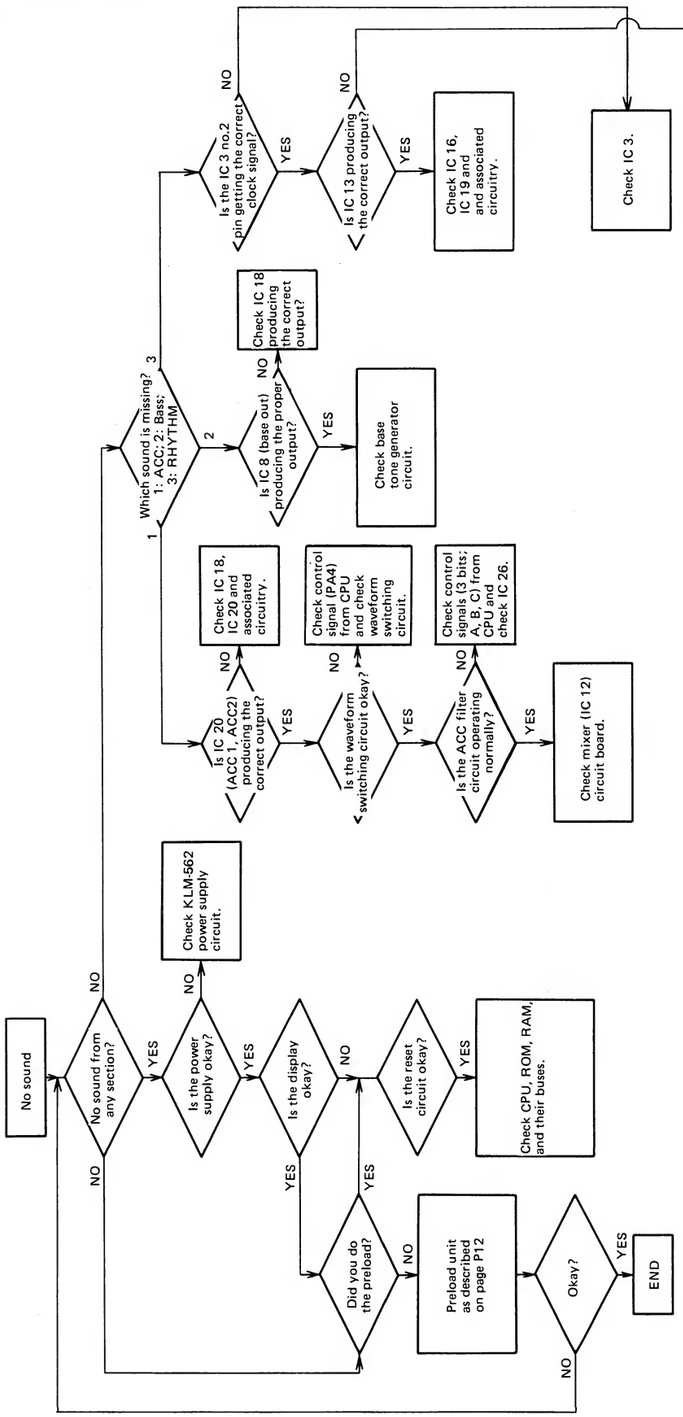
Symbol	Function
DB0 ~ B7	Data input terminals. Connected to CPU data bus, so all data is input through these terminals.
AB0 ~ AB3	Address input terminals. These inputs select data write registers.
ALE	When this input is at "H", trailing edge is latched and signals applied to AB0-AB3 are input to address register.
WR	When this input is at "L", trailing edge is latched and signals applied to DB0-DB7 are input to data latch.
CLK1, CLK2	Reference clock input. Output scale is obtained by frequency division of this input. CLK1 is the reference frequency for tone generators TG0-TG3 (group 1), while CLK2 is for TG4-TG7 (group 2).
RST	Internal initialization input terminal. Pull-up resistor is built in.
CAP0-CAP7	Envelope generator capacitor connection terminals. Envelopes are generated by charging and discharging of this capacitance through internal resistance. Furthermore, if envelope generator operation is prohibited, a high impedance state will be created and external envelope waveform input will become possible.

Symbol	Function
2'-1 ~ 16'-1, 2'-2 ~ 16'-2	Tone bus output terminals. Divided into group 1 and group 2. Each is made up of four registers: 2', 4', 8', and 16'. Four tone generators are connected to each tone bus, and are mixed by current adding. Therefore this output must be fed to a low impedance.
SOLO8', SOLO16'	Solo sound source output terminals. TG7, 8' and 16' pitched rectangle waves are always available at these outputs.
GATE	On/off signal output for solo outputs. In the solo mode, TG7 GF is output. It becomes "L" level when solo mode is prohibited.
NO	Noise output terminal. Internal simulated random noise generator provides noise which is available at this output at all times.
VDD1, VSS1	5 V power supply terminal.
VDD2, VSS2, VSS3	5 ~ 15 V power supply terminal.

NOTE: Please connect VDD1 and VDD2 as well as VSS2 and VSS3, each externally.

7. TROUBLESHOOTING TABLE

CAUTION:
Use a 10:1 probe of oscilloscope. Erratic operation may occur with a 1:1 unit. Be particularly careful when checking the CPU. Malfunction may occur if you touch the wrong part of the CPU with a probe or other tool. In such cases, turn the unit off and then turn the power back on again.



8. CHECK & ADJUSTMENT PROCEDURE

Test Procedures

Before testing, always SAVE data to tape then VERIFY saved data to ensure against loss of user created memory contents.

Next use the PSS-50's internal preload function as described below.

Hold down the ENTER, FUNCTION, PATTERN, and CHORD switches all at once and then turn the power switch off and then on again. Or hold down the same switches and then shift the TAPE switch from DISABLE toward FROM and then back to DISABLE again. The display will show "Pr Ld" and all functions will be reset to factory default conditions.

1. MODE switch check.

Turn the MODE switch from the POWER OFF position to the ARRANGE position, one step at a time while checking for the following indications.

BATT CHECK	:	b - 6d
TUNE	:	- 7U
SONG CHAIN	:	1 c01
PLAY	:	d 71
WRITE	:	1 01
ARRANGE	:	A -

2. Panel push switch check.

Set MODE to SONG CHAIN.

1) Press ENTER and confirm that the number in the CHAIN STEP/BAR NO. display increases one at a time.

2) Press CLEAR and confirm that the CHAIN STEP/BAR NO. display decreases one at a time.

3) Press Aug while holding down FUNCTION. Confirm that this has the same effect as pressing ENTER.

4) Press dim while holding down FUNCTION. Confirm that this has the same effect as pressing CLEAR.

5) Confirm that the display changes when PATTERN/SONG is pressed.

6) With the pattern display on, press keys C through B one at a time in order. Confirm that the displayed chord name and pitch match the keys played.

7) Press m through sus4. Check displayed chord name and sounded chord.

8) Press CHORD and PATTERN switches. Check that both LEDs go out.

9) Confirm proper operation of COUNT START/RHYTHM FILL-IN and START/STOP switches.

10) Connect foot switch (S-2 type) to inputs on rear panel and confirm same operation as in (9) above.

3. Stereo output mix.

Set MODE to TUNE and connect R/MIX output to amplifier.

Press switches m through sus4 to check drum sounds.

Connect a dummy plug to the L output and confirm that the 7 and 9 drum sounds are now not output from the R/MIX jack.

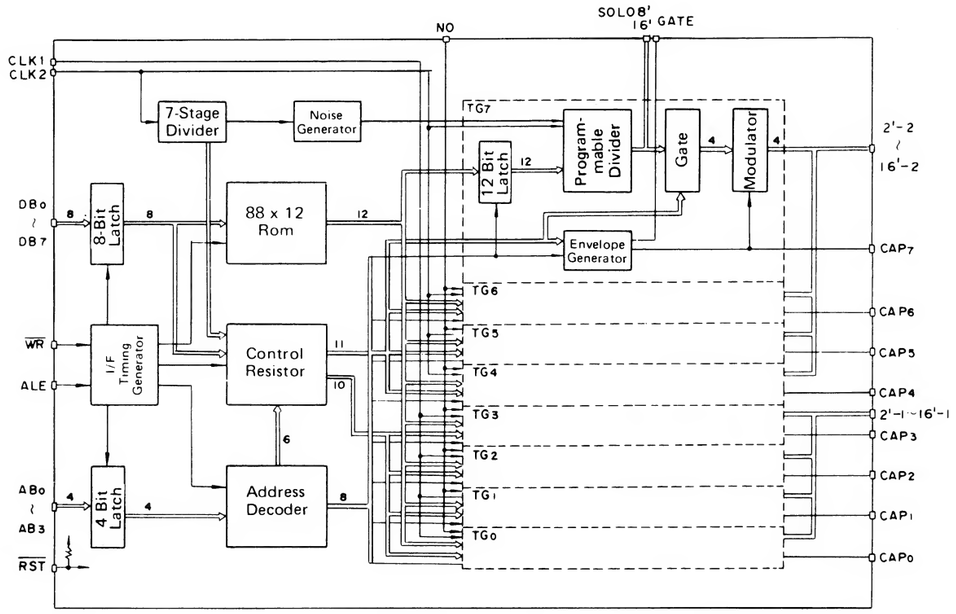
NEXT, connect L output to amplifier, and connect a dummy plug to the R/MIX output and confirm that the dim, Aug, and sus 4 drum sound are now not output from the L output jack.

NOTE:

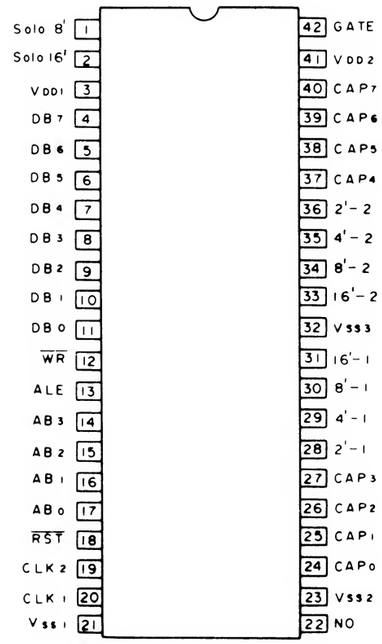
Check rhythm section functions while in this mode. Use oscilloscope connected to R/MIX output. (Check timbre, level, etc.)

IC MSM5232RS 8 CHANNELS MUSICAL INSTRUMENT TONE GENERATOR

BLOCK DIAGRAM



PIN CONFIGURATION

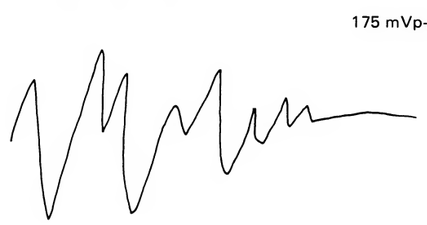


FUNCTIONAL PIN DEFINITION

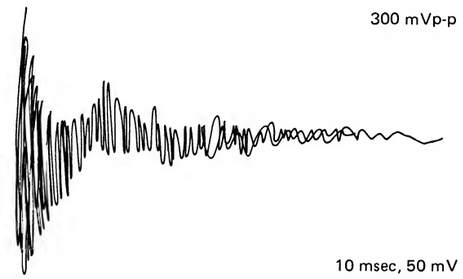
Pin No.	Name	Code	Function
2	Shift pulse	C	Shift register shift pulse
15	Data input	D_1	Shift register data input shift pulse rising edge memory
1	Strobe	S	Outputs shift register contents on "1"
12	Output	O_0	Register contents change from "1" to "9" when 1st bit is output.
11	Output	O_1	Register contents change from "1" to "0" when 2nd bit is output.
10	Output	O_2	Register contents change from "1" to "0" when 3rd bit is output.
9	Output	O_3	Register contents change from "1" to "0" when 4th bit is output.
8	Output	O_4	Register contents change from "1" to "0" when 5th bit is output.
7	Output	O_5	Register contents change from "1" to "0" when 6th bit is output.
6	Output	O_6	Register contents change from "1" to "0" when 7th bit is output.
5	Output	O_7	Register contents change from "1" to "0" when 8th bit is output.
3	Data output	D_0	Takes C_7 output for input to next stage.
16	Power supply	Vcc	Normally uses 5.0V (±10%).
13	Ground	GND_1	Ground for $O_0 \sim O_3$ output circuit.
4	Ground	GND_2	Ground for $O_4 \sim O_7$ output circuit.
14	Ground	GND (Dig)	Logic circuit ground.

NOTE:
GND_1 and GND_2, pins 13 and 14 are grounded internally.

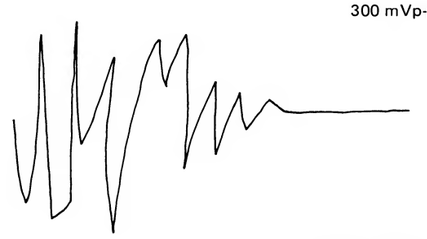
m BASS DRUM
175 mVp-p
10 msec, 50 mV



6 RIM SHOT
300 mVp-p
10 msec, 50 mV

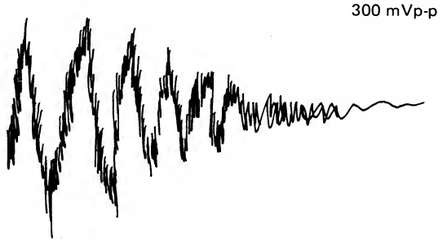


m6 BASS DRUM
300 mVp-p
10 msec, 50 mV

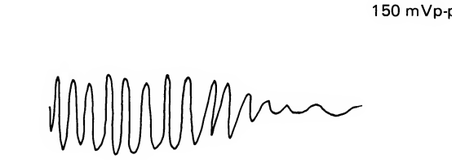


7 HIGH TOM
150 mVp-p
20 msec, 50 mV

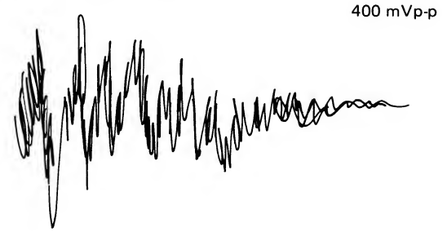
m7 SNARE DRUM
300 mVp-p
10 msec, 50 mV



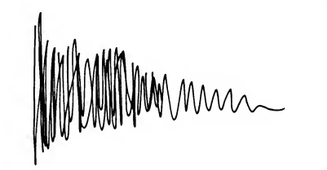
Maj7 LOW TOM
150 mVp-p
20 msec, 50 mV



m9 SNARE DRUM
400 mVp-p
10 msec, 50 mV



9 HAND CLAPS
150 mVp-p
20 msec, 50 mV



dim CLOSED HI-HAT

80 mVp-p

20 msec, 50 mV

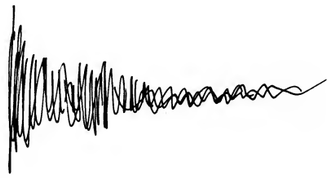
sus4 OPEN HI-HAT

90 mVp-p

50 mV, 20 msec

Aug CLOSED HI-HAT

120 mVp-p



20 msec, 50 mV

ADJUSTMENT PROCEDURE

CAUTION:
This unit was precisely adjusted at the factory. Never adjust anything other than those points that require it.

1. Master oscillator check and adjustment.

Set MODE to TUNE, ACCOMP volume to MAX, and TUNE control to center. Connect a callibrated AT-12 chromatic tuner to the R/MIX jack.

1) Press A key. For A, the AT-12 should indicate A ± 0 cents at the 0 active. Adjust coil L1 on KLM-562 if necessary.

2) Next, turn the TUNE control from the flat to the sharp position and confirm that the range is ± 40 cents or more but no greater than ± 70 cents. Adjust VR1 if necessary then check tuning and range again.

2. Stereo circuit, BBD, and bias check and adjustment.

Set MODE selector to TUNE, press A key.

1) Use oscilloscope to check Stereo VR (VR7 no.3 pin, figure 1). Confirm that signal amplitude is at the maximum. Adjust VR10 if necessary.

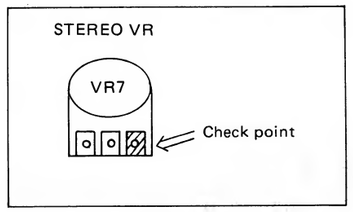
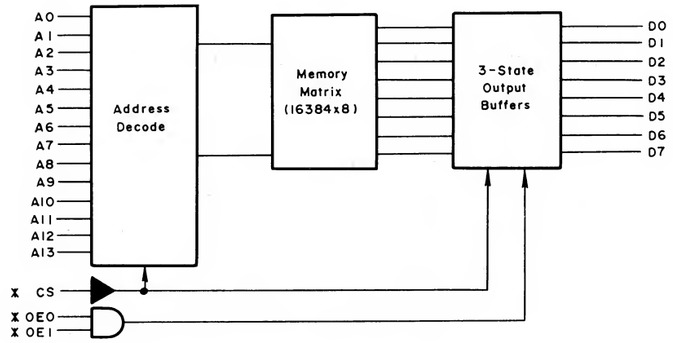


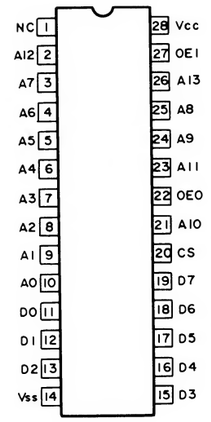
Figure 1

HN61328P 8-BIT CMOS MASK PROGRAMMABLE READ ONLY MEMORY

BLOCK DIAGRAM

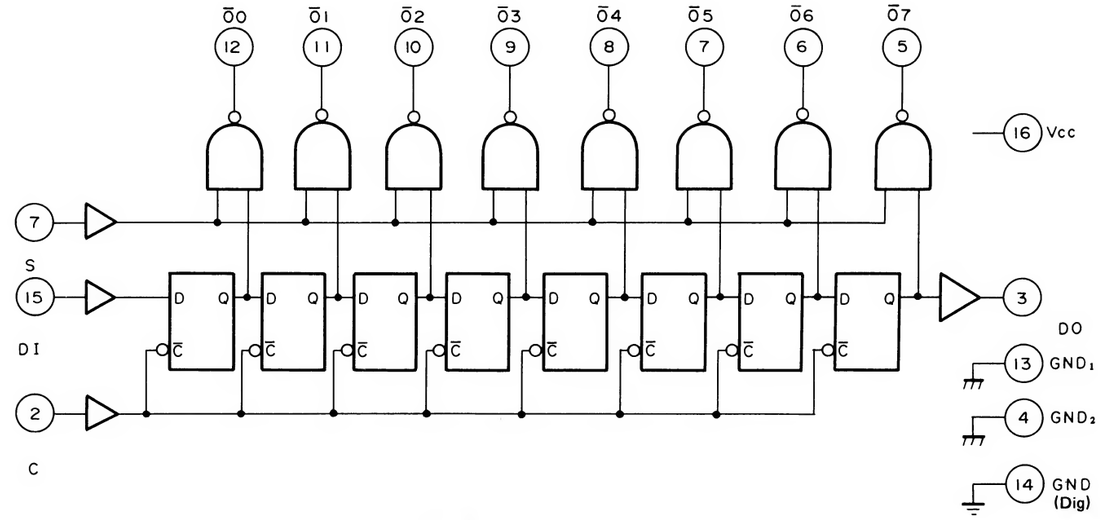


PIN CONFIGURATION

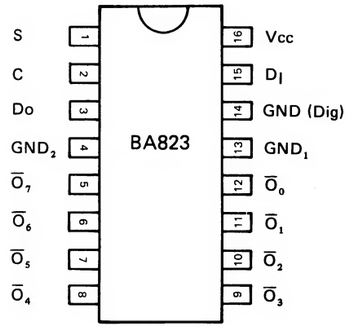


BA823 8-BIT SERIAL IN PARALLEL OUT DRIVER

BLOCK DIAGRAM



PIN CONFIGURATION



1.13 / out (Clock Output) Output.
Output for system clock frequency (1/4 of internal quartz oscillator frequency or X1 external-1 clock frequency). Output continues in the hold mode but stays at high in the stop mode.

1.14 SCK (Seriral Clock) Tristate output.
An IO serial data control clock. Outputs the internally generated clock signal when the internal serial clock mode is selected. Inputs an external serial clock when the external serial clock mode is selected.
Serial register (S/P) register contents are output with the MSB first to the SO terminal with the SCK trailing edge. With the SCK rising edge, SI terminal data is latched in the serial register.

1.15 SI (Serial Input) Input.
A serial input port. SI line serial data is latched to the serial register with the SCK leading edge. MSB is first.

1.16 SO (Serial Output) Output.
A serial output port. Serial register data is output through the SO terminal with the SCK trailing edge. The MSB is first.

1.17 REL (Release Stop Mode) Input.
Standby function stop mode release input. The stop mode is released by raising the REL input to high. This also makes the clock oscillator circuit resume functioning. The standby control register bit 3 (SC3) is set (1) when REL input is high and is reset when it returns to low (0). Has internal pull-down resistor.

1.18 RESET (Reset) Input.
System is reset with input of 8 μs (at 4 MHz operation) or longer low level input. This results in the following defaults:

* All mask register bits are set.
* Interrupt enable flags are reset to prevent interrupts.
* All interrupt request flags are reset so any held requests are eliminated.
* All mode B register bits are set so port B becomes input.
* Serial register bit 6 (SM6) is set so serial clock becomes external mode.
* Standby control register bit 3 (SC3) is reset and the other bits are set. The hold mode and stop mode are both released.
* PSW are all reset (0).
* 0000H is loaded into program counter (PC).
* Timer circuit prescaler and up counter are cleared.
* All TIMER REG bits are set (to FFH).
* All timer mode register (TMM) bits are set, TO output goes to low, and PRESCALERO goes to input mode.
* All port A output goes to low level.
* The data bus (DB7 ~ DB0) goes to high impedance.
* So terminal goes to low level.
* WR & RD signals go to high level.
* Other CPU register contents become unpredictable.

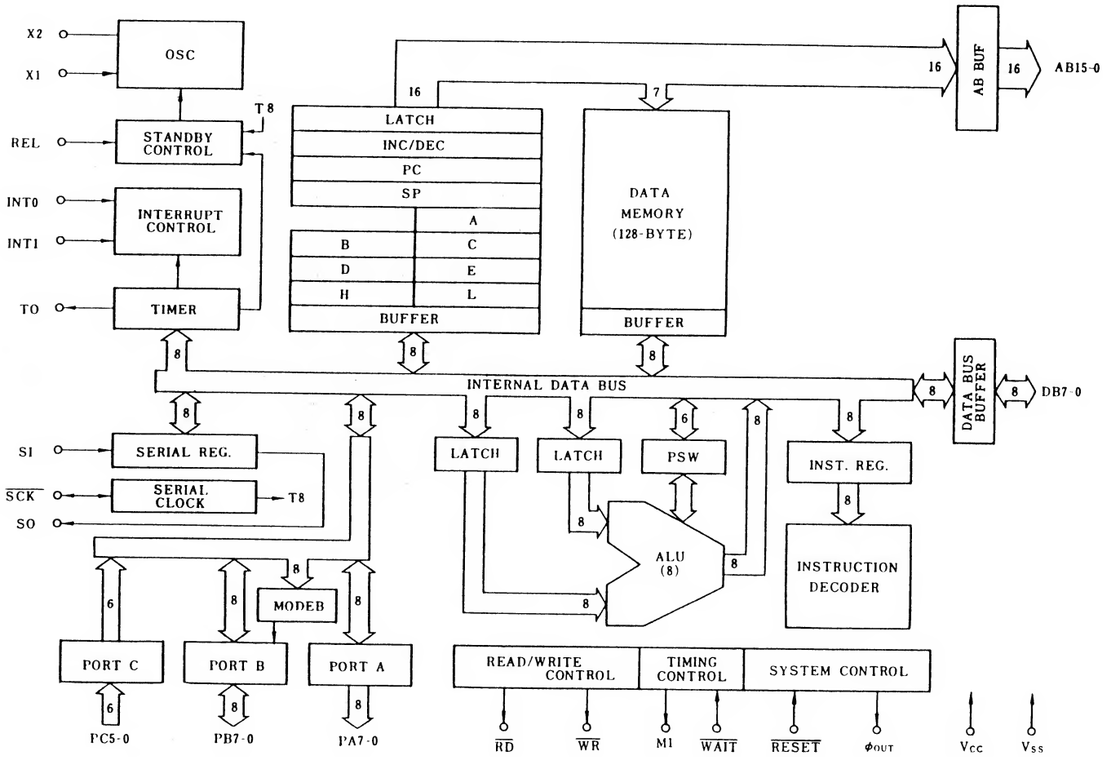
To prevent malfunction due to noise, the RESET input is sampled with an internal clock cycle of 4 μs so that level changes of 4 μs or less are ignored. Therefore, it is necessary to keep it at low level for 8 μs or longer with async in order to be received. When the RESET input goes to high level, the program starts at 0000H.

9. REFERENCE DATA

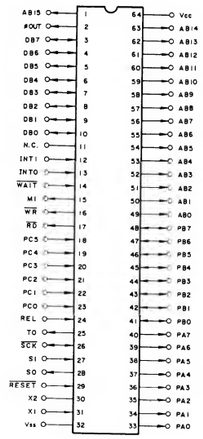
CPU μPD78C05G

The μPD78C05G is an 8-bit microprocessor with ALU, RAM, and IO ports on one chip. It can address up to 64K of external memory, RAM or ROM, directly. A standby function reduces power consumption. The μPD78C05G has functions compatible with and can be used as an evaluation chip for the μCOM-87LC (μPD78C06G).

BLOCK DIAGRAM



PIN CONFIGURATION



Terminal functions

1.1 PA7-0 (Port A) Output.
An 8-bit output port with latch function. Data can be moved between the latch and the accumulator by using movement instructions. Latch contents can be set using arithmetic instructions. Data written to the latch remains unchanged until a new command is executed for port A or it is reset. Output level is TTL.

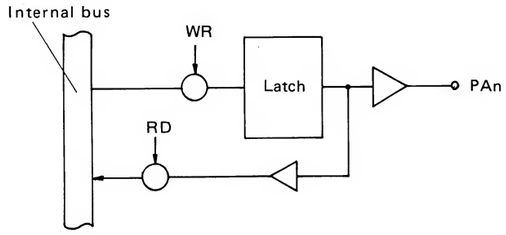


Figure 1-1 Port A.

1.2 PB7-0 (Port B) Tristate IO port.
8-bit input/output port with latch on output only. Port B can be selected for input or output in bit units depending on the mode B register. Output goes to high impedance when selected as the input port or reset. Input level is CMOS level. Output level is TTL.

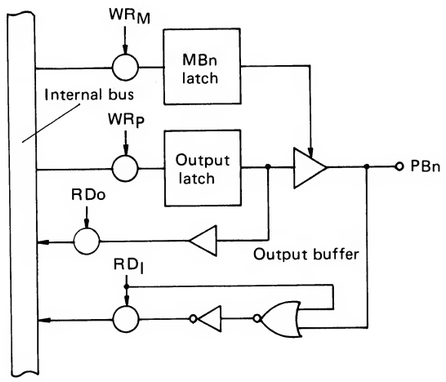


Figure 1-2a Port B.

(a) When selected as output port (MODE Bn = 0).
The output latch becomes effective and data can be moved between the accumulator and the latch by using movement instructions. Output latch contents can be set using arithmetic instructions. Output latch contents remain unchanged until the next command for port B is executed or it is reset.

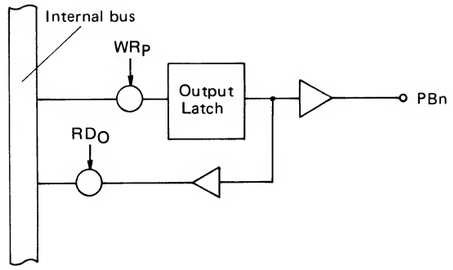


Figure 1-2C Port B selected as input port.

(b) When selected as input port (MODE Bn = 1).
PB (port B) line contents can be loaded into the accumulator by using movement instructions. In this case it is still possible to write to the output latch and data transmitted from the accumulator will be stored in the output latch regardless of whether the port is selected for input or output.
However, the output latch contents of bits specified for input ports cannot be loaded to the accumulator or output to the terminal since the output buffer is set to high impedance (working as an input terminal). Data stored in the output latch in this way can be output to the external terminal and loaded to the accumulator when the bit is switched to output.

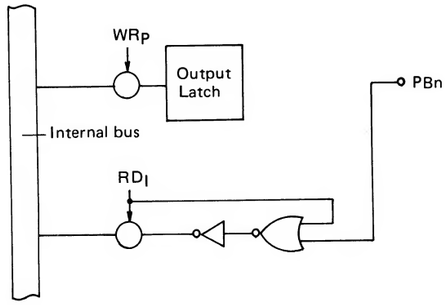
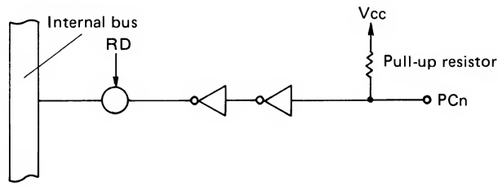


Figure 1-3 Port C.

Actual commands are executed in 8-bit units. If there is a port B read (MOV A, PB) command, the contents of the input line of the port selected for input and the contents of the output latch of the port selected for output will be loaded into the accumulator. With a port B write command (MOV PB, A, for example), it will be performed on both the output latch of the port selected for input and that of the port selected for output, but output latch contents of the port selected for input will not be output to the external terminal.

1.3 PC5-0 (port C) Input.
A 6-bit, pull-up resistor equipped input port. This port's input data can be tested with bit test instructions or can be loaded into the accumulator's least significant six bits with movement commands. Input level is CMOS level. Suitable for use as a key input port.



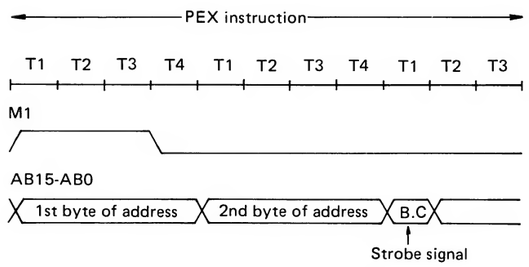
1.4 WR (Write Strobe) Output.
Strobe signal output when writing data to external memory. High level when inactive.

1.5 RD (Read Strobe) Output.
Strobe signal output when reading data from external memory. High level when inactive.

1.6 TO (Timer Out) Output.
Outputs square wave at half cycle of internal timer count. Goes to low level immediately following reset.

1.7 DB7-DB0 (Data Bus) Tristate IO.
An 8-bit bidirectional data bus for external memory (and IO). Goes to high impedance in input mode, hold mode, stop mode, and following reset. Input and output are TTL level.

1.8 AB-15-AB0 (Address Bus) Output.
A 16-bit address bus for accessing memory addresses 0-65, 407, including μPD78C05G internal ROM (0-4, 095) area. Unlike the μPD78C06, this does not have port functions (it has no latch). When the port E operation (PEX) instruction is executed, the BC register pair contents are output only in the first clock cycle space after the ninth clock cycle after execution begins (third machine cycle T1 state), in between addresses. PEX instruction execution timing is as shown in the following diagram.



With the μPD78C05G it is not possible to obtain PEX instruction discrimination codes or strobe (STB) signals like the μPD7800. Therefore, to use BC data externally, sample the data bus externally during instruction fetching, decode the data to determine PEX instructions, count clock cycles to produce strobe signals, and latch the data.

1.9 MI (Machine Cycle) Output.
This output signal informs the outside world that this is the first machine cycle of an instruction. High level is output for T1 ~ T3 of the number 10P code fetch cycle.
Used for latch control of BC data during fetch instruction execution and instruction stop and break operation.

1.10 Wait (Wait Request) Input.
This can be used to prolong read/write timing by using a low level signal input when external memory (or IO) access time is slow.
The wait signal is checked in place of T2 and the wait state is entered if it is low. TW is repeated until the wait signal goes high. Has internal pull-up resistor.

1.11 IN0 INT1 (Interrupt Request) Input.
Takes external interrupt requests with INT0 for a level trigger and INT1 for an edge trigger. Priority is as shown. INTT is internal timer interrupt.

IN0 > INTT > INT1

(i) INT0.
The high level active level trigger interrupt input; has highest priority.

(ii) INT1.
The leading edge interrupt input; has lowest priority. Effective when INT1 goes from low to high. Therefore, after reception of an initial INT1 interrupt it is necessary to raise the INT1 input to high after a low period in order to be able to receive the next INT1 interrupt.

To prevent malfunction due to noise, both interrupt inputs are sampled with an internal clock cycle of 1 μs (operating at 4 MHz) so that noise of 1 μs or less is removed.
Therefore, it is necessary to keep the interrupt request active (high level) for 2 μs or more for INT0 or INT1.

1.12 X2, X1 (Crystal).
Connection for oscillator for internal clock. If clock is provided from outside, it is input to X1. X1 input level is CMOS level. The oscillator frequency or external clock is divided by 4 to yield the system clock.